UNIVERSITY OF WATERLOO
Faculty of Engineering

E&CE 437:
Integrated VLSI Systems

4-bit Transmission Gate Ripple Carry Adder for Low Power Consumption Design

Prepared by:

Yen Pin Hsiao
Ian Hung

March 26, 2004

Table of Contents

Table of Contents 2
List of Figures 3
List of Tables 4
List of Tables 4
Abstract 5
Abstract 5
1.0 Introduction 5
1.1 Project Requirements 6
1.2 Target Application and Parameters 6
2.0 Functional and Architectural Design 6
2.1 Functional Requirements 7
2.2 Architecture Selection 7
2.3 Architecture Design 7
2.4 Performance Metrics and Design Methodology 8
3.0 Circuit Design and Simulation 9
3.1 Low Power Optimization of Circuit Design 11
3.1.1 Low Power Optimization of Transmission Gate 11
3.1.2 Low Power Optimization of Inverter 14
3.1.3 Glitch Reduction 15
3.2 Simulation of Schematic 19
4.0 Physical Layout 21
4.1 CMOS Sizing 22
4.2 Simulation of Layout 24
5.0 Analysis 27
5.1 Comparison of Schematic with Layout 27
5.2 Comparison of Layout with Target Application 27
6.0 Conclusion 29
References 30

List of Figures

Figure 1: 4-Bit TG Ripple Carry Adder 9
Figure 2: Test Bench of 4-bit TG Ripple Carry Adder 10
Figure 3: TG Implementation of Full Adder 10
Figure 4: Test Bench of TG Full Adder 11
Figure 5: Test Bench of TG for Device Power 12
Figure 6: Parametric Analysis of TG 12
Figure 7: Transient Response of TG for Device Power 13
Figure 8: Inverter Schematic 14
Figure 9: Parametric Analysis of Inverter 14
Figure 10: Transient Response of Inverter 15
Figure 11: Transient Response of 4bit Adder before Optimization for Glitch 16
Figure 12: Transient Response of 4bit Adder after Optimization for Glitch by Increasing Load Capacitance 17
Figure 13: Transient Response of 4-bit Adder after Optimization for Glitch by Carry Path Speedup 17
Figure 14: Transient Response of Final 4-bit Adder Schematic 19
Figure 15: Transient Response of Final 4-bit Adder Schematic 19
Figure 16: Full Adder Layout 21
Figure 17: 4-Bit TG Ripple Carry Adder Layout 21
Figure 18: NMOS Layout Measurements 22
Figure 19: PMOS Layout Measurements 23
Figure 20: Contact Measurements 23
Figure 21: Simulation of Extracted Layout before Adjustment 24
Figure 22: Simulation of Extracted Layout after Adjustment 25

List of Tables

Table 1: Technical Specifications of the GBA 6
Table 2: Comparison of 4-bit Parallel Adders 7
Table 3: Transmission Gate simulation Data 13
Table 4: Inverter simulation data 15
Table 5: Glitch Reduction Simulation Data 18
Table 6: Schematic Simulation Data 20
Table 7: Layout Area and Size 23
Table 8: Layout Simulation Data 25
Table 9 : Comparison of Schematic simulation data and Layout simulation data 27
Table 10: Comparison between 4-bit TG Adder Performance with Target Application 28

Abstract

The objective of this report is to design a parallel 4-bit adder for low power consumption using 0.18 micron technology. The transmission gate implementation of the 4-bit ripple carry adder is chosen. Implementation is based on a bottom-up design methodology from schematic design of individual devices to integration. Critical paths are abstracted and optimized for low power dissipation. The schematic design is translated into prefabrication layout. Simulation of the schematic and layout realizations of the adder is performed and results are discussed. Performance is validated with specifications imposed by the target application.

1.0 Introduction

The parallel adder is the most important element used in arithmetic operations of many processors. With the rising popularity of mobile devices, low power consumption and high performance integrated circuits has been the target of recent research. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other. Design for low power consumption and high performance is further complicated by the myriad of factors that are introduced through the development life cycle of the digital processor. Development is based on a five-tier model: System Integration, Algorithm Selection, Architectural Design, Circuit/Logic Design, and finally, Process Technology. This project shall focus on the Circuit/Logic Design level. Design at this level is restricted by the given process technology.

The objective of this project is to design a 4-bit adder that is optimized for low power consumption. However, it should be noted that power dissipation optimization should be applied throughout the development process from system-level to process-level while realizing that performance is still essential. In reality, it is very important to know the power distribution within a processor and optimize the parts of blocks consuming an important fraction of the power. In the case of this report, the process technology and circuit/logic design is under the control of the designer. The other levels are acknowledged but will be considered negligible in the power analysis of this report with respect to the target application. It is assumed that as long as power consumption by the 4-bit adder falls below the constraints of the target application within a certain fraction, therefore the design objectives are met.

The 4-bit adder design is completed in the following manner: the target application is first chosen; next, the adder architecture is selected for its appropriateness for that application. The architecture is analyzed by tracing the worst-case path for power dissipation and sections of the design are abstracted for optimization. Finally, the schematic design of the adder is translated into layout and its performance metrics are compared with those from the schematic as well as the target application.

1.1 Project Requirements

The project requirement is to design a 4-bit adder for low power consumption. Operating voltage should be approximately 1.8V or less. The process technology given is 0.18 microns. Schematic design and layout are carried out using Cadence. Simulation is based on the SpectreS model.

1.2 Target Application and Parameters

The target application of the adder is to become an integral instruction of the processor found in mobile gaming devices such as the Gameboy Advance (GBA). Technical specifications of the device are widely available and are representative of many similar mobile products available today. The specifications of the GBA are listed in the table below.

Table 1: Technical Specifications of the GBA

Performance Metrics	Technical Specifications
CPU	32-bit RISC-CPU + 8-bit CISC-CPU
Power Supply	2 AA Batteries [Ni-Cd 1.25V/1000mAh]
Expected Days of Operation	15 hours
Operating Frequency	16 MHz
Operating Voltage	<3V

The specifications of the mobile console form a guide for our initial adder design. As stated earlier, the adder alone cannot account for the overall power consumption of the processor but rather it is a fraction of the overall power that is consumed by all levels of the design including other components beyond the integrated circuit; for instance, powering the TFT or the production of sound. Therefore, by simply defining the number of hours the GBA may operate due to the power consumed by the adder is false since it is impossible to evaluate power consumption that is solely due to the adder. Rather, the performance metric imposed by the GBA forms a lower bound to the values resulting from the adder. Thus, it can be assumed that by satisfying the number of hours in operation at a certain margin greater than expected (at a lower voltage), it can be stated that the design is adequate or better than the original specifications. Moreover, the project is restricted to 4-bit addition which is not very practical for most applications since any basic computation would exceed the functional capacity of the adder. Perhaps the adder may be cascaded to obtain greater functionality; in which case, power consumption and delay for a single 4-bit block must be minimal. Therefore, the aim of the 4-bit adder design is to obtain absolutely the lowest power dissipation possible considering the narrow scope of the adder relative to the rest of the components for the target application.

2.0 Functional and Architectural Design

This section of the report identifies the functional requirements of the project. The appropriate architecture is selected for the target application in satisfying the project

objectives and justified. Next, the nuances and critical paths of the design are stated. Lastly, the performance metrics and design methodology are described in evaluating the design.

2.1 Functional Requirements

This severely limits the performance of the adder. There are many ways to construct the n-bit adder; however, this will be examined in the following section. The functional requirement of the adder is to be able to perform unsigned addition of two 4-bit numbers in parallel. Power consumption must also be minimal.

2.2 Architecture Selection

The propagation of the carry in a n-bit adder is inevitable. This property is important since it can severely impact adder performance. Hence, there are various implementations of the parallel adder available each with its own tradeoff in terms of power and delay. The different architectures are compared below:

Table 2: Comparison of 4-bit Parallel Adders

This architecture is selected because of the following reasons: compared to the symmetrical implementation of RCA, the carry signal only passes through one TG; thus, this circuit may be potentially faster and have lower power dissipation since the effects of glitching, an output of spurious transitions, may be minimized. The TG implementation also simplifies the overall design of the 4-bit adder because the output or inputs do not require an inverter for correct logical operation of the subsequent full adder. Either the static symmetrical RCA or TG variant consumes the least power and occupy the smallest area of all parallel adder designs according to preliminary research. Since delay is a secondary objective for our desired application, the TG implementation of the RCA is considered the most appropriate architecture.

2.3 Architecture Design

The Transmission Gate implementation of the Ripple Carry Adder is selected as the primary architecture for this project. The carry bit ripples through the n-stages and the sum of the nth bit cannot be performed until the carry C_n-1 is evaluated. The delay of the n-bit addition is given by $t_{rca}=(n-1)t_c + ts$ such that t_c and t_s is the sum delay. Consequently, the carry propagation path is the critical stage for the delay. The sum and carry out functions are given below:

$$S = A \oplus B \oplus C \quad (1)$$

$$C_{out} = AB + (A + B)C_{in} \quad (2)$$

In practice, the carry bit signal diminishes every 4 1-bit stages; therefore, an inverter is added every four stages to reduce the signal degradation due to the distributed ripple carry effect. When the carry signal is inverted, the complementary carry path adder is used for the next 4-bit stages. The critical path is identified to be the bottom-most path which passes through the transmission gate since Cout is driven by the carry signal from the preceding full adder.

2.4 Performance Metrics and Design Methodology

A set of performance metrics is devised to consistently record simulation data. The following performance metrics listed are initial parameters to be controlled in the test bench before simulation: Voltage supply (V_{dd}), Load Capacitance, Input Rise Time, Input Fall Time, and Input Frequency. In addition, minimum widths and lengths for both the NMOS and PMOS are used and varied only when stated. Oppositely, the following post simulation performance metrics are collected: Rise Time, which is the time required for the signal to rise from 10% to 90% of V_{dd}; Fall Time, defined as the time required for the signal to drop from 90% to 10% of V_{dd}; Average Input Power, power dissipation due to inputs since the output of the TG adder are driven by the inputs under certain circumstances; Average Device Power, power dissipation required for the device to function since occasionally the output of the TG adder is driven by the voltage source of the device; Power Dissipation, which is the sum of average input and device power; Delay, the time for the signal to travel from the input to C_{out} of the final stage of the adder; Power Delay Product, the value calculated from multiplying power and delay; Maximum Frequency, calculated by the equation (1/(4*td)); and finally, the Figure of Merit, obtained by the equation (Frequency/Power). These are the default performance metrics used in the report unless otherwise stated.

A bottom-up design methodology is adopted in the development of the 4-bit TG adder. The fundamental components are first designed and optimized such as the transmission gate and inverter. Secondly, the components are integrated together into a final schematic and optimization using various techniques that shall be mentioned in their respective sections of this report is performed. Thirdly, the design is translated into a layout and simulation is once again conducted. Lastly, simulation data from the layout is compared with data obtained from the schematic.

3.0 Circuit Design and Simulation

Shown in Figure 1 below is the schematic of the 4-bit TG ripple carry adder. Each block represents a 1-bit TG implementation of the full adder. There are four stages in total such that the initial carry bit of the first 1-bit full adder block is set to ground. In addition, the design is abstracted into a symbol. The test bench is displayed in Figure 2.

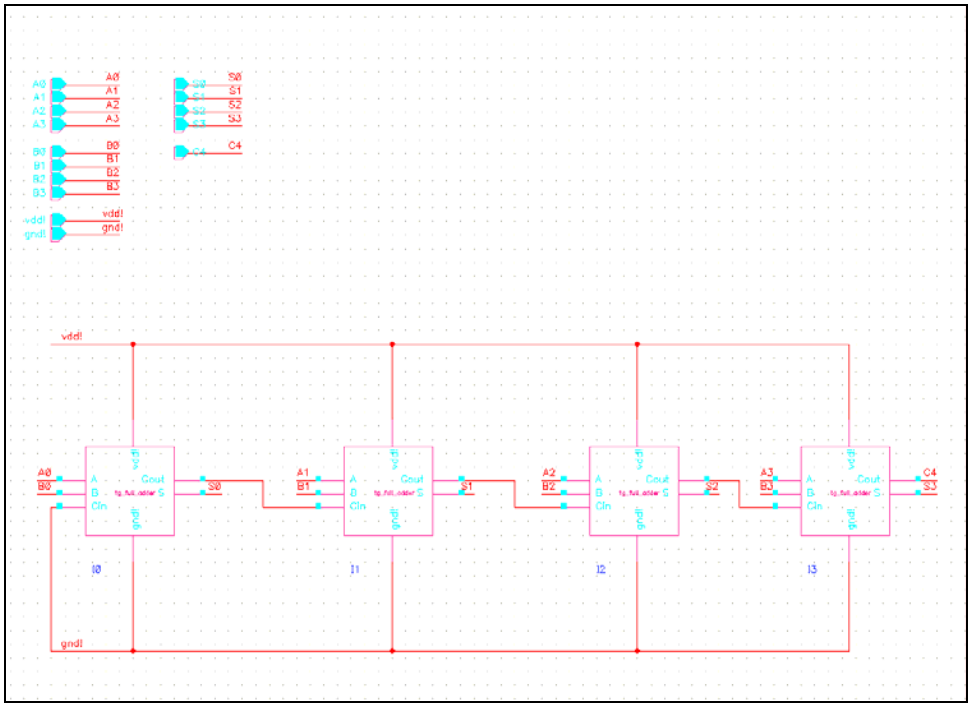

Figure 1: 4-Bit TG Ripple Carry Adder

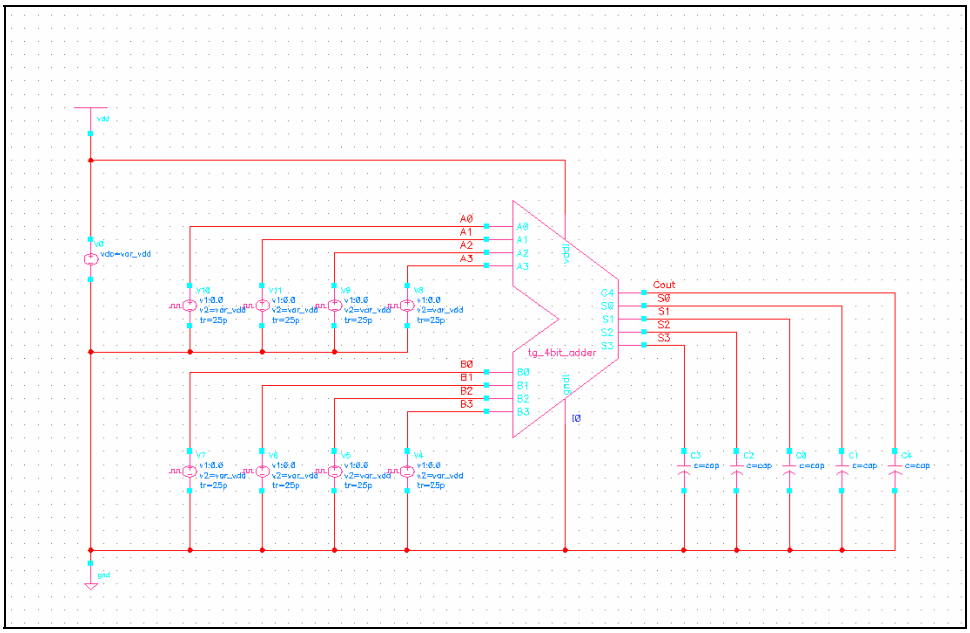

Figure 2: Test Bench of 4-bit TG Ripple Carry Adder

The schematic of the 1-bit Transmission Gate Full Adder Block is illustrated in Figure 3 along with its corresponding test bench in Figure 4.

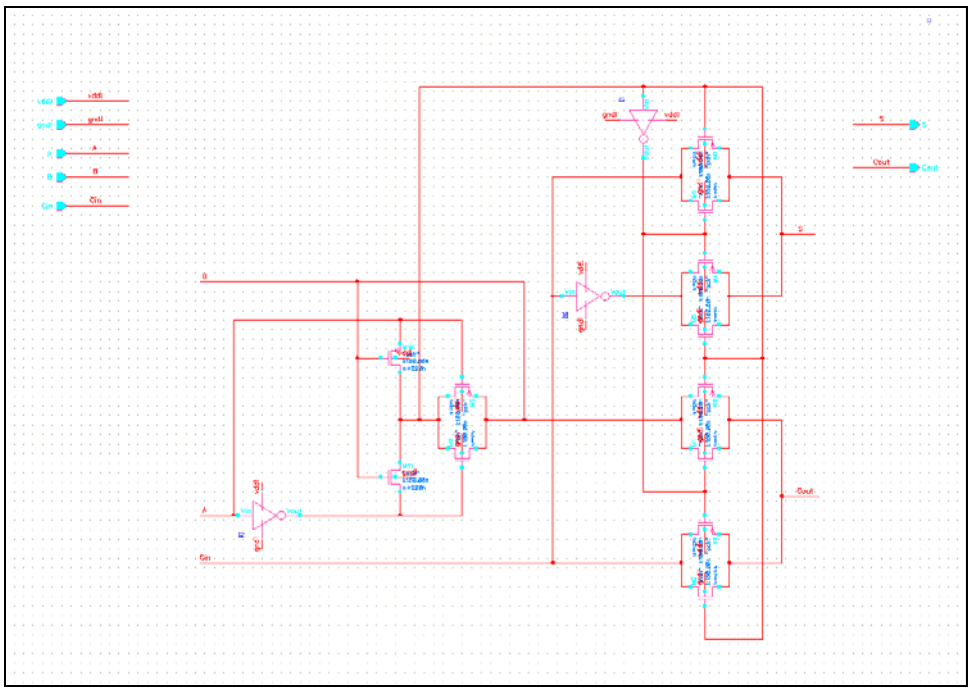

Figure 3: TG Implementation of Full Adder

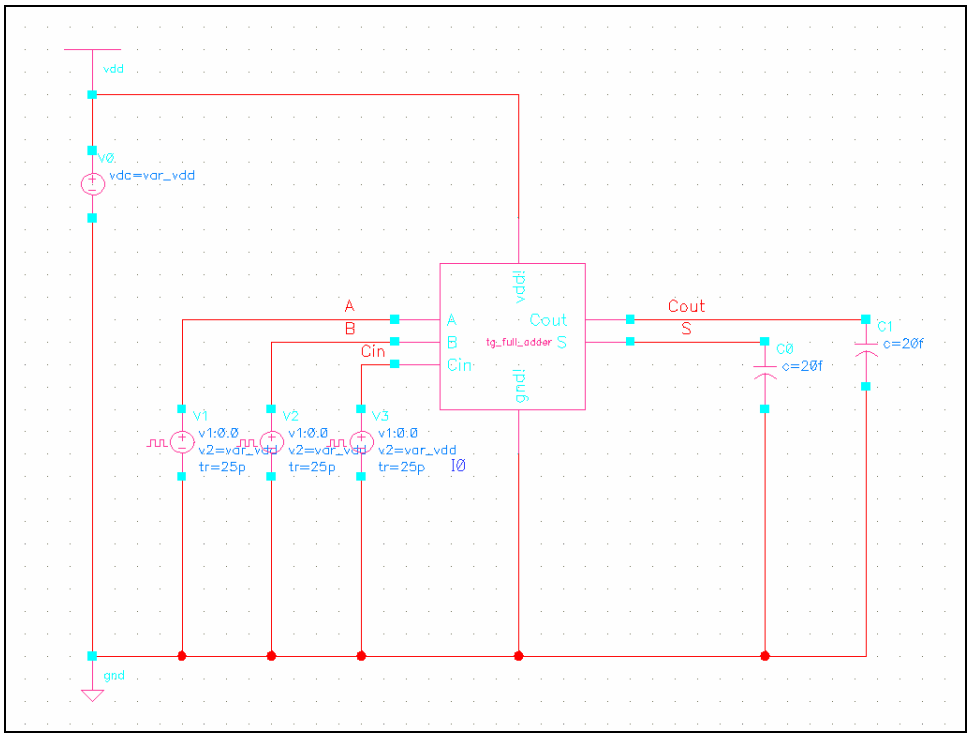

Figure 4: Test Bench of TG Full Adder

3.1 Low Power Optimization of Circuit Design

A column of transmission gates occupy the final stage of the full adder; and thus, it is of utmost importance that power dissipation is minimized for each transmission gate at the atomic level while keeping delay at a reasonable value. In addition, under certain situations, the voltage source of the inverter may be driving the outputs of the full adder; hence, that particular component must be optimized as well. Optimization of these parts is discussed respectively in the next sections.

3.1.1 Low Power Optimization of Transmission Gate

Our 4-bit adder design consists mostly on transmission gates, it is therefore essential to investigate the technique of optimizing power on transmission gates. Figure 5 below shows the schematic of our transmission gate test bench. There are two transmission gates in the figure, when the input signal is low; it turns on the gate on top to charge up the output. Similarly, when the input signal is high; it turns on the gate on the bottom to discharge the output. Notice there are two voltage sources in this schematic, voltage source, V4, is used to power up the device and voltage source, V1, is used to drive the input signals.

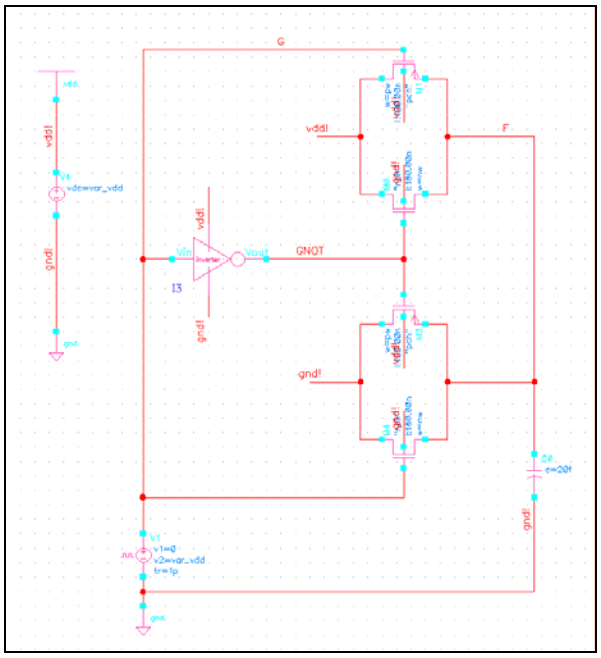

Figure 5: Test Bench of TG for Device Power

A parametric analysis on varying the PMOS transistor width was done to observe the power consumption. The result is shown in Figure 6, it is observed that power consumption is the least when we have minimum size for both NMOS and PMOS. The power for the transmission gate devices goes up rapidly as the width of PMOS increases.

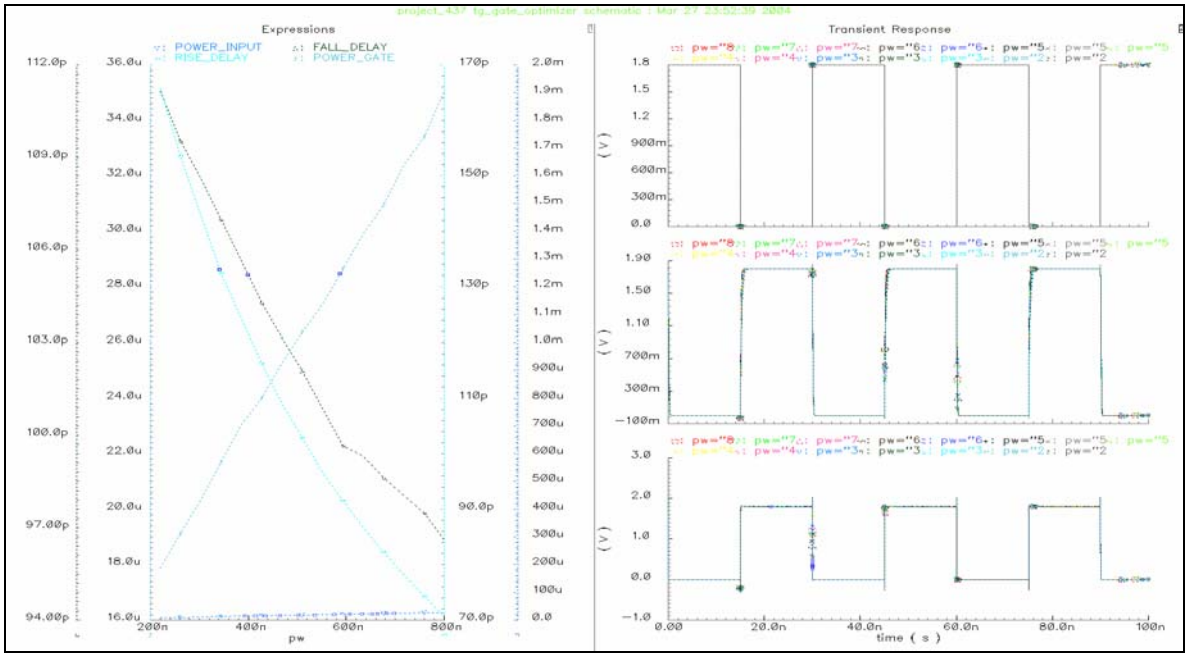

Figure 6: Parametric Analysis of TG

Figure 7 below shows the transient analysis of the transmission gate output. The delay is around 165ps. The maximum operating frequency is about 1.5GHz. These values and the values of rise time, fall time and power are also summarized in Table 3.

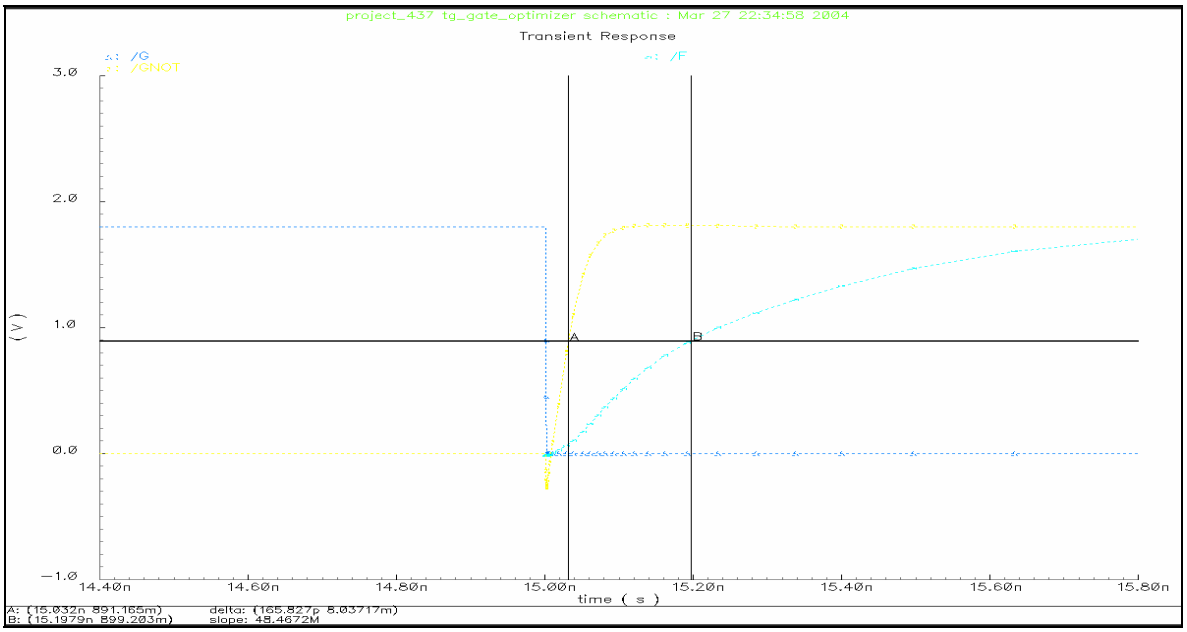

Figure 7: Transient Response of TG for Device Power

Table 3: Transmission Gate simulation Data

Controlled Variables:

Variable	Value
Vdd	1.8v
Load Capacitance	20f
Input Rise Time	1p
Input Fall Time	1p
Minimum Width	220n
Minimum Length	220n
Input Frequency	33Mhz
Simulation Time	100n

Observation:

Variable	Value
Rise Time	165.8p
Fall Time	111.2p
Average Input Power	8.17u
Average Device Power	17.89u
Power Dissipation	26.06u
Delay	165.82p
Power Delay Product	4.32f
Maximum Frequency (1/4*td)	6.03GHz (1.507GHz)
Figure of Merit (Frequency/Power)	2.31exp14

Parametric Analysis

Variable	Value
PMOS width	220n-800n 20 steps

3.1.2 Low Power Optimization of Inverter

Similarly, it would be handy to observe the technique for optimizing inverter since there are two inverters in each full adder design. Figure 8 shows the schematic of the inverter design. By varying the width of the PMOS transistor from 220nm to 800nm, we can observe that both input power and device power go up as the width increases. The result is shown in Figure 9.

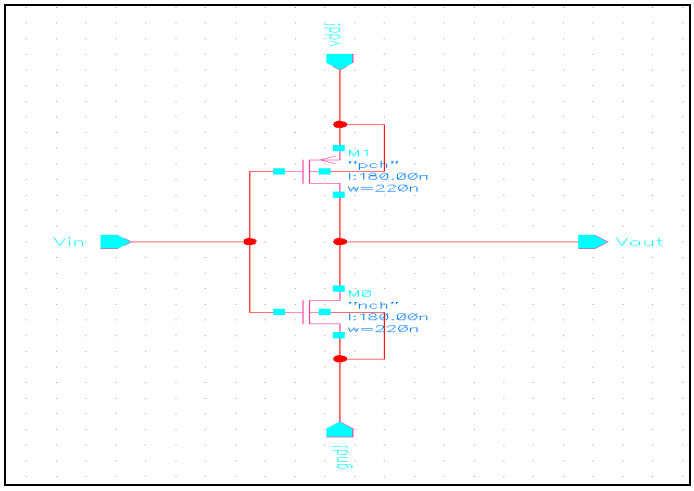

Figure 8: Inverter Schematic

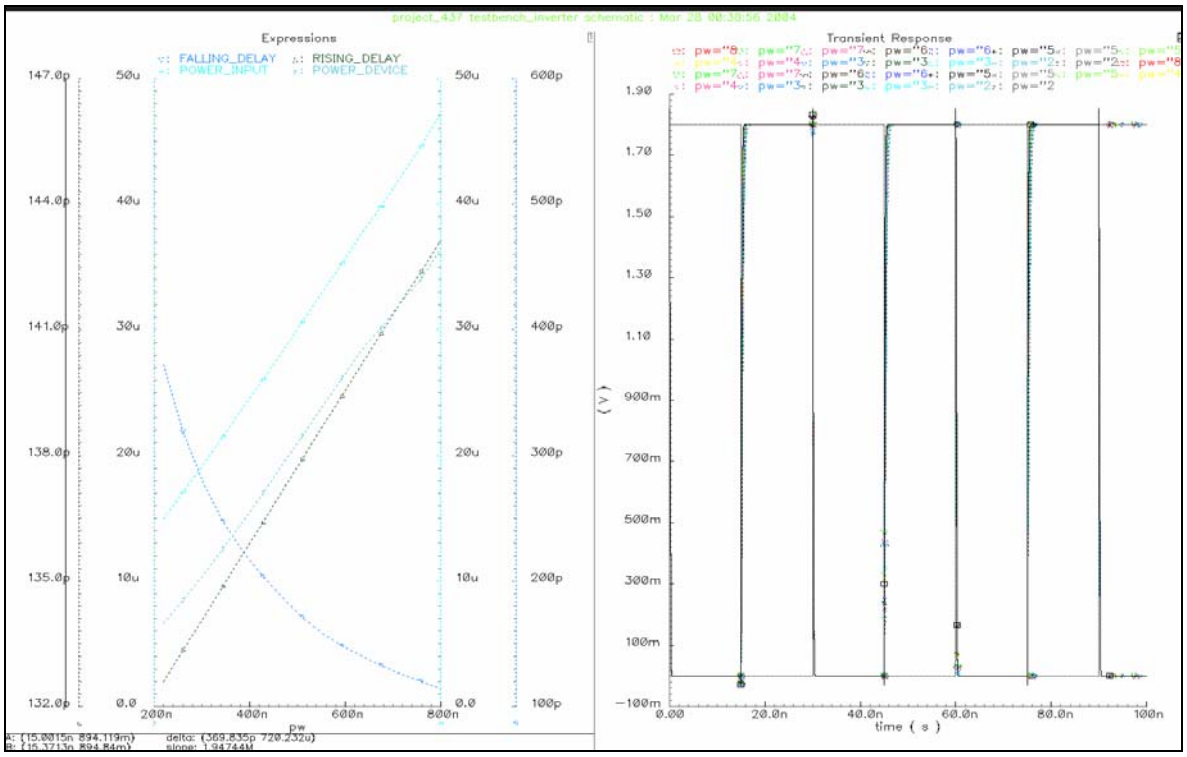

Figure 9: Parametric Analysis of Inverter

Figure 10 below shows the transient analysis of the inverter. The delay is around 369.8p. The maximum operating frequency is about 676MHz. These values and the values of rise time, fall time and power are also summarized in Table 4.

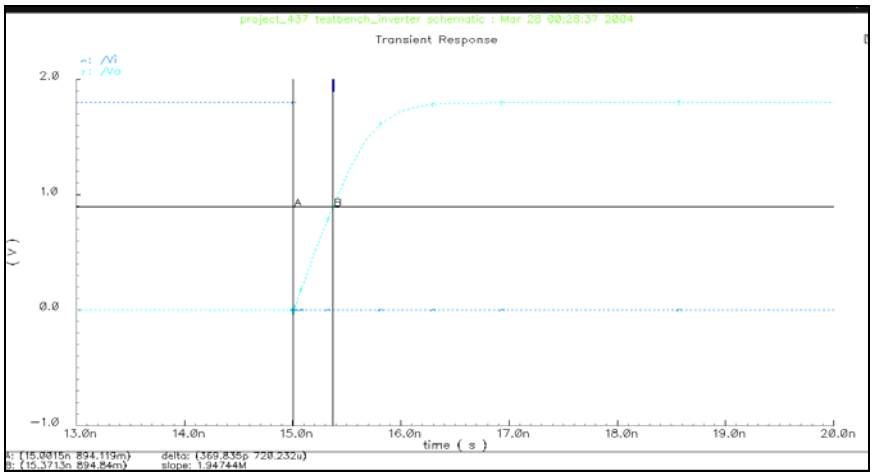

Figure 10: Transient Response of Inverter

Table 4: Inverter simulation data

Controlled Variables:

Variable	Value
Vdd	1.8v
Load Capacitance	20f
Input Rise Time	1p
Input Fall Time	1p
Minimum Width	220n
Minimum Length	220n
Input Frequency	33Mhz
Simulation Time	100n

Observation:

Variable	Value
Rise Time	132.6p
Fall Time	372.2p
Average Input Power	14.97u
Average Device Power	6.639u
Power Dissipation	21.609u
Delay	369.836p
Power Delay Product	7.99f
Maximum Frequency (1/4*td)	675.9MHz
Figure of Merit (Frequency/Power)	31.28x10^12

Parametric Analysis

Variable	Value
PMOS width	220n-800n 15 steps

3.1.3 Glitch Reduction

The 4-bit adder consists of four full adders in sequence. Each full adder depends on the C_{in} feed in from the previous adder. As a result, there is a propagation delay on C_{out} path. The

propagation delay causes input signals on the full adders arrive at different time. This phenomenon causes glitches in the design to occur; the glitches are shown in the simulation result in Figure 11. To achieve the goal of minimizing the power consumption, it is essential to try to reduce glitches.

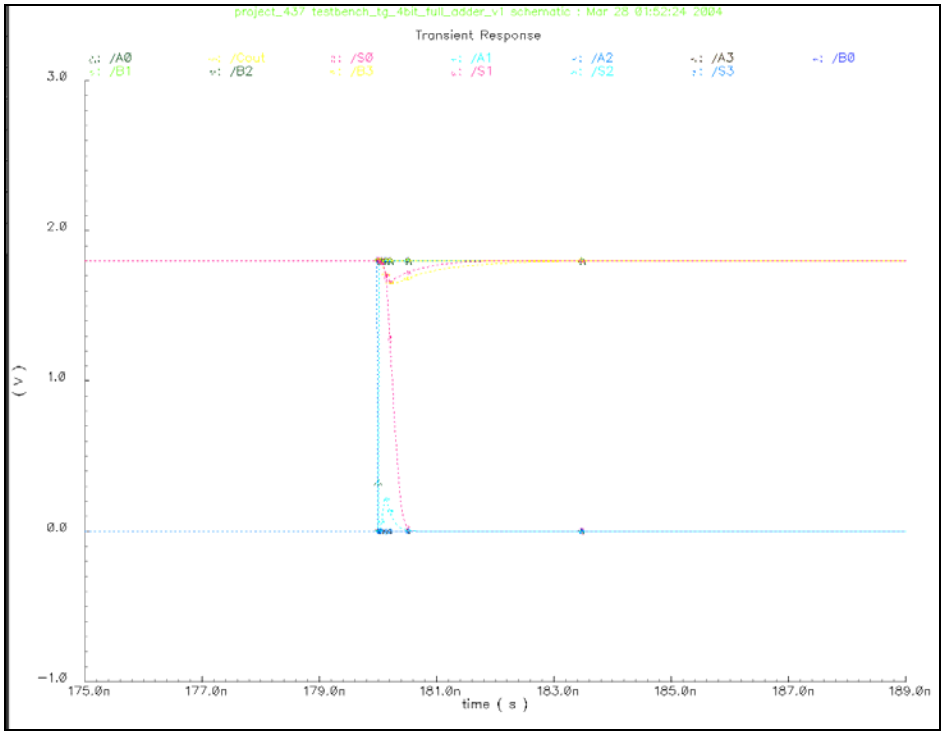

Figure 11: Transient Response of 4bit Adder before Optimization for Glitch

This section focuses on the attempts to reduce glitches as to reduce power consumption. The first attempt is to speedup the C_{out} path by increasing the width of the PMOS and NMOS transistors that are associated with the C_{out} path. The PMOS width was sized to 800nm and the NMOS width was sized to 300nm. The simulation result is shown in Figure 12 and the values are summarized in Table 5. The glitch length is shortened slightly but the glitch voltage increases.

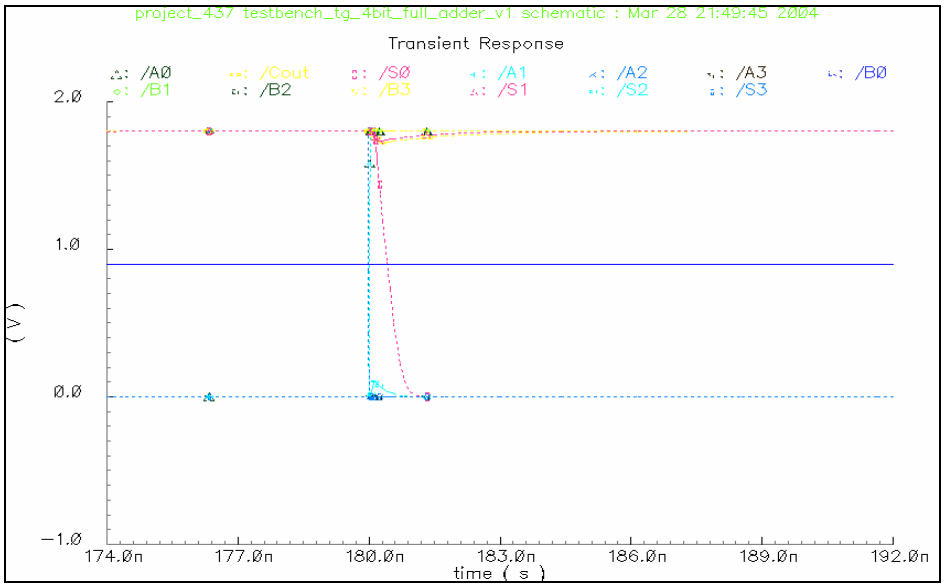

Figure 12: Transient Response of 4bit Adder after Optimization for Glitch by Increasing Load Capacitance

The second attempt to reduce glitch phenomenon is to increase the output capacitance. The output capacitance is changed from 20fF to 50fF. The simulation result is shown in Figure 13 and the values are summarized in Table 5. As expected, the glitch voltage does not drop/rise as much and increasing the capacitance makes the glitch length longer because it takes more time to charge up the capacitance. Hence, the power dissipation also increases. This is further proven by the power dissipation value in the table.

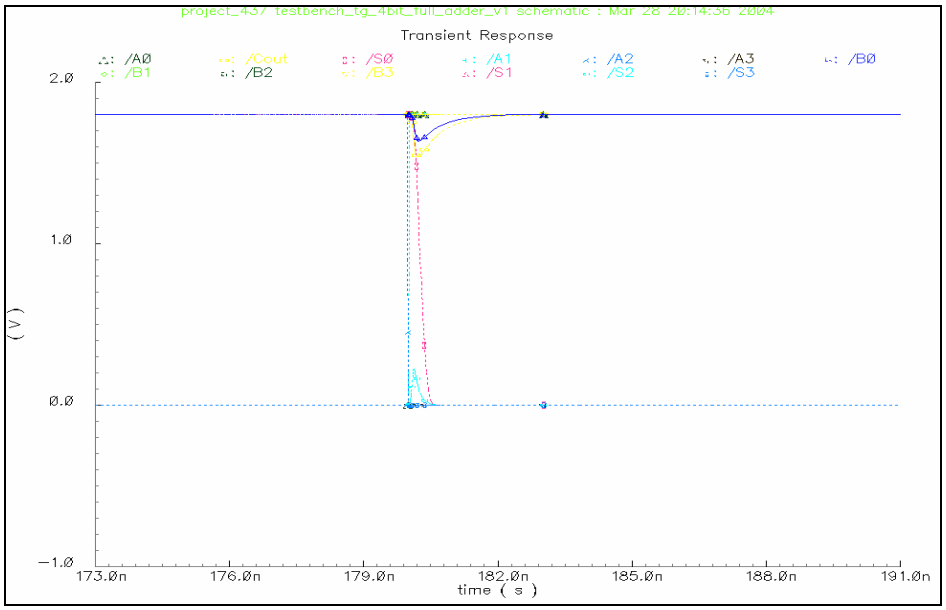

Figure 13: Transient Response of 4-bit Adder after Optimization for Glitch by Carry Path Speedup

Table 5: Glitch Reduction Simulation Data

Controlled Variables:

Variable	Value
V_{dd}	1.8v
Load Capacitance	20f
Input Rise Time	1p
Input Fall Time	1p
Minimum Width	220n
Minimum Length	220n
Input Frequency	33Mhz
Input Value Frame of Capture	
Simulation Time	500n

Observation:

Variable	Base Value	Speedup Cout	Increase Cap
Rise Time	167p	162.5p	389.4p
Fall Time	210.6	205.5p	554.93p
Average Input Power	8.515u	7.31u	8.09u
Average Device Power	9.655u	10.31u	14.92u
Power Dissipation	18.17u	17.62u	23.01u
Delay	317.89p	307.5p	510.42p
Power Delay Product	5.77f	5.41f	1.17x10^-14
Maximum Frequency (1/4*td)	786.4MHz	813 MHz	498.58MHz
Figure of Merit (Frequency/Power)	43.2x10^12	46.14 x10^12	21.67x10^12

Glitch min V

	Base				Speed up Cout Path				Increase Load capacitance			
	Falling		**Rising**		**Falling**		**Rising**		**Falling**		**Rising**	
Signal	**Voltage (mV)**	**Delay (ns)**	**Volt (mV)**	**Delay (ns)**	**Voltage (mV)**	**Delay (ns)**	**Volt (mV)**	**Delay (ns)**	**Voltage (mV)**	**Delay (ns)**	**Volt (mV)**	**Delay (ns)**
S0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
S1	**1662**	**0.892**	**210.7**	**0.3109**	**1636**	**0.5341**	**250.9**	**0.3057**	**1734**	**1.595**	**101.6**	**0.8574**
S2	**1665**	**0.8881**	**216.4**	**0.49638**	**1585**	**0.624**	**224.9**	**0.2872**	**1735**	**2.303**	**106**	**0.418**
S3	**1621**	**2.5662**	**301.4**	**0.33965**	**1607**	**1.939**	**222.7**	**0.2643**	**1633**	**7.08**	**129.9**	**0.9314**
C_{out}	**1697**	**1.189**	**-**	**-**	**1539**	**0.7251**	**-**	**-**	**1724**	**1.9246**	**-**	**-**

Another possible technique to reduce glitches is to delay the input signal on the second, third and the fourth full adder to make the input and C_{in} signals arrive at the full adders at the same time. Due to the limited human resource and the complexity of the design, a schematic for this technique is not generated.

In conclusion, there is a tradeoff using either the first or the second technique. It is decided to stay with the original minimum size design since the effects of glitches are negligible to logical function of adder.

3.2 Simulation of Schematic

The results from the final simulation of the 4-bit Transmission Gate adder schematic is shown in Figure 14 and Figure 16. The latter figure shows a closer look at the transient response for the purpose of observing the effects of glitching while the former figure shows an overall transient response of the circuit for a fraction of the input combinations.

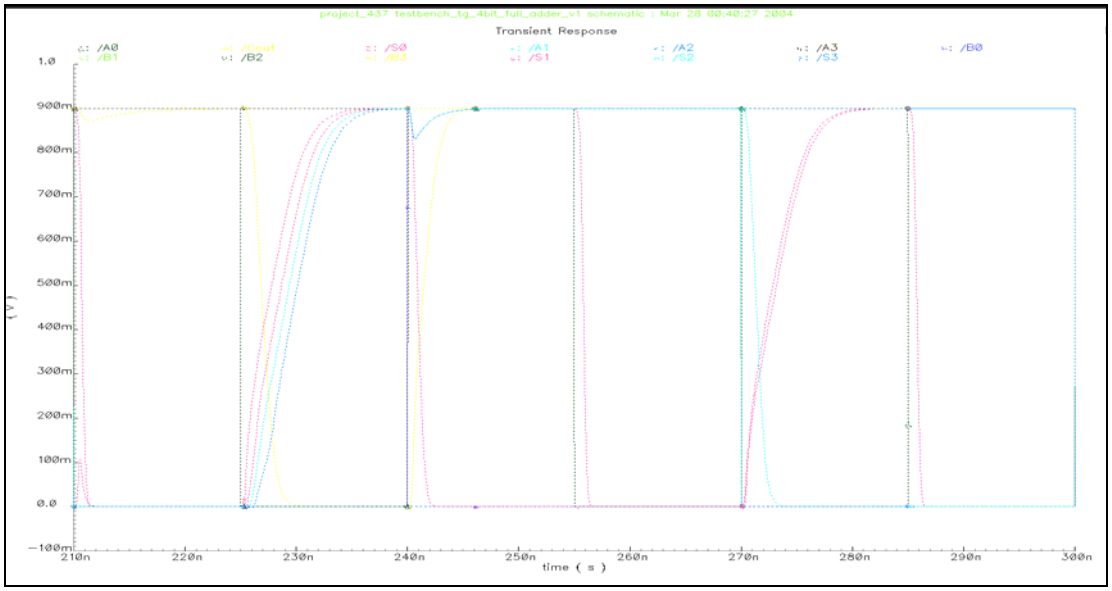

Figure 14: Transient Response of Final 4-bit Adder Schematic

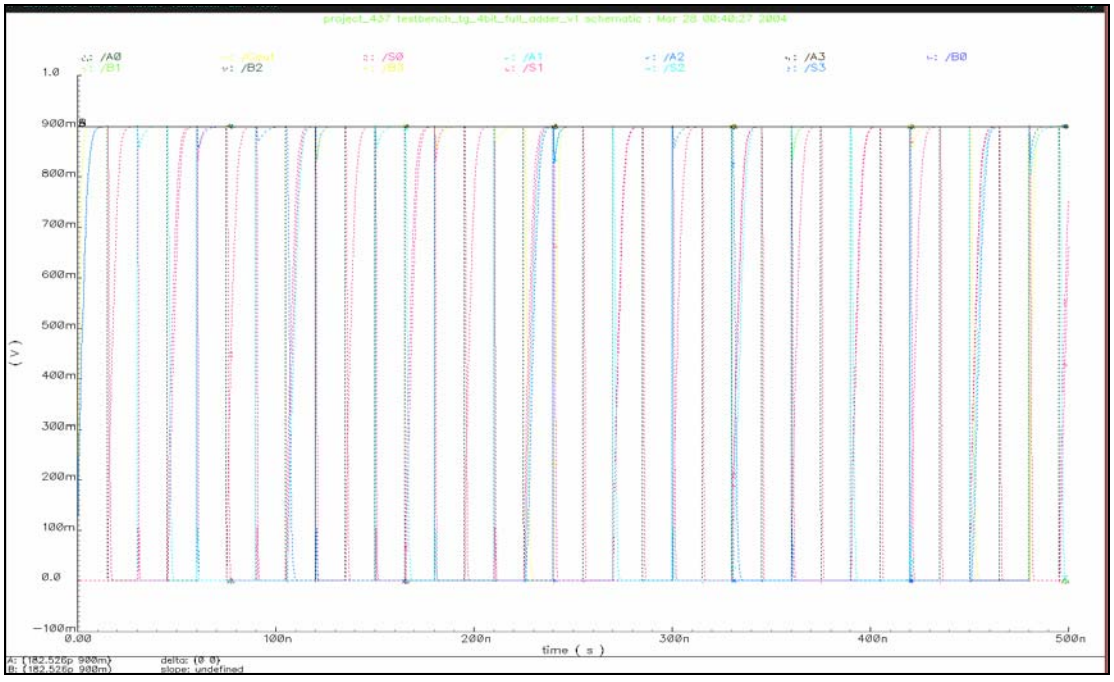

Figure 15: Transient Response of Final 4-bit Adder Schematic

The results of the simulation along with the initial input parameters are listed in the Table Table 6 below.

Table 6: Schematic Simulation Data

Controlled Variables:

Variable	Value
V_{dd}	0.9v
Load Capacitance	20f
Input Rise Time	1p
Input Fall Time	1p
Minimum Width	220n
Minimum Length	220n
Input Frequency	33Mhz
Simulation Time	3840n

Observation:

Variable	Value
Rise Time	777p
Fall Time	734.97p
Average Input Power	0.9215u
Average Device Power	1.729u
Power Dissipation	2.6505u
Delay	3.263n
Power Delay Product	8.64f
Maximum Frequency (1/4*td)	76.6MHz
Figure of Merit (Frequency/Power)	28.9 x10^12

Glitch min V

	Falling		Rising	
Signal	**Voltage (mV)**	**Delay (ns)**	**Volt (mV)**	**Delay (ns)**
S0	**-**	**-**	**-**	**-**
S1	**832**	**3.982**	**100.8**	**1.094**
S2	**831**	**5.08624**	**100.2**	**0.942**
S3	**831**	**5.08624**	**100.2**	**1.03**
C_{out}	**870.7**	**4.47172**	**97.8***	**0.856***

The effects of glitching can be observed in the 4-bit full adder design. With an input frequency of 33Mhz, glitching appear to be minimized since there is sufficient time for the signal to stabilize. As mentioned in the previous section, the degree of glitching may be attributed to various factors that directly impact the critical path of the circuit. Although the rise and fall time of glitching may be reduced and/or the severity of the spikes minimized, this occurs at the expense of power dissipation. In the interest of minimal power dissipation, it is found that minimum transistor sizing provided the least amount of power dissipation with fair glitching response. In particular, the operational frequency at 33mHz ensures that the correct value has propagated throughout the circuit by the time the next input is supplied. Hence, minimal sizing of transistors throughout the 4-bit TG adder is considered acceptable in this regard.

4.0 Physical Layout

The 4-bit TG adder schematic is translated into pre-fabrication layout. The design methodology employed is once again bottom-up. The layout of the 1-bit full adder block is completed and tested first before integration into the final 4-bit adder. This is shown respectively on Figure 16 and Figure 17.

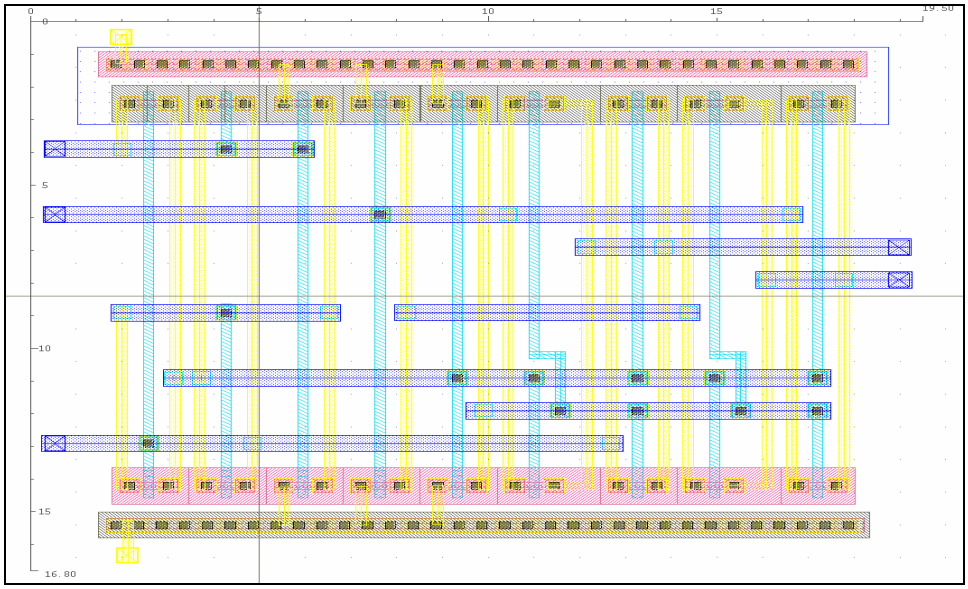

Figure 16: Full Adder Layout

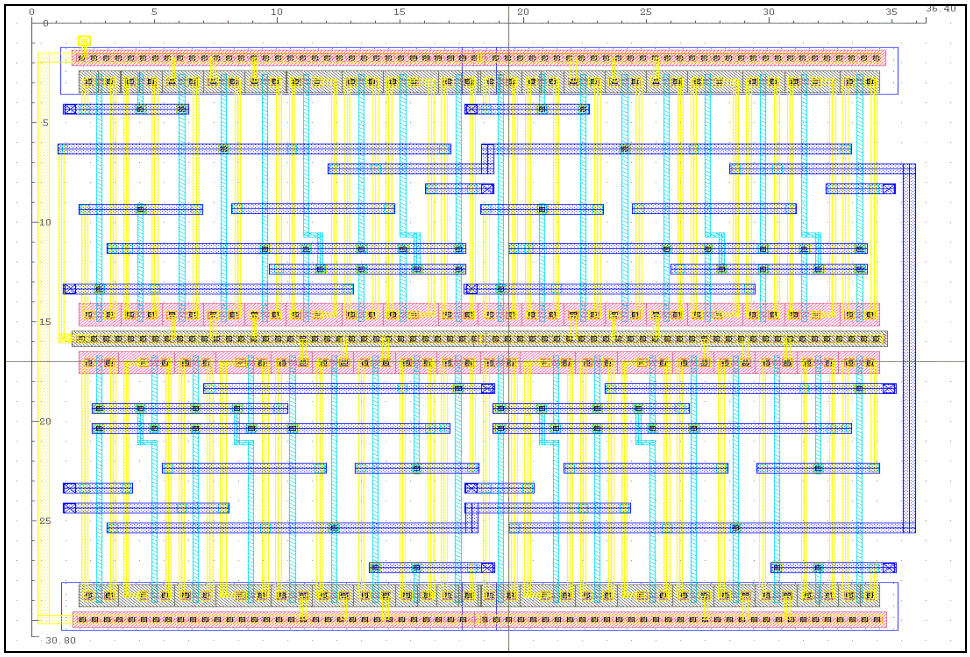

Figure 17: 4-Bit TG Ripple Carry Adder Layout

4.1 CMOS Sizing

The channel dimensions of the CMOS are of particular interest when translating the schematic into layout since this factor can seriously influence the performance of the circuit. For low power consumption, minimum channel widths and lengths are utilized as indicated in Figure 18, Figure 19 and Figure 20 below. However, the drain and source contacts require a surrounding active region with distance greater than the width of the channel; therefore, a "Dog Bone"-like transistor is revealed. Delay may be critically affected by the width and length ratio of this setup. Since minimum dimensions are used in the schematic with positive results, the same dimensions are chosen under the confidence that, although the simulation results may slightly degrade due to various parasitic effects inherent of the layout, the general waveform and performance should be expected.

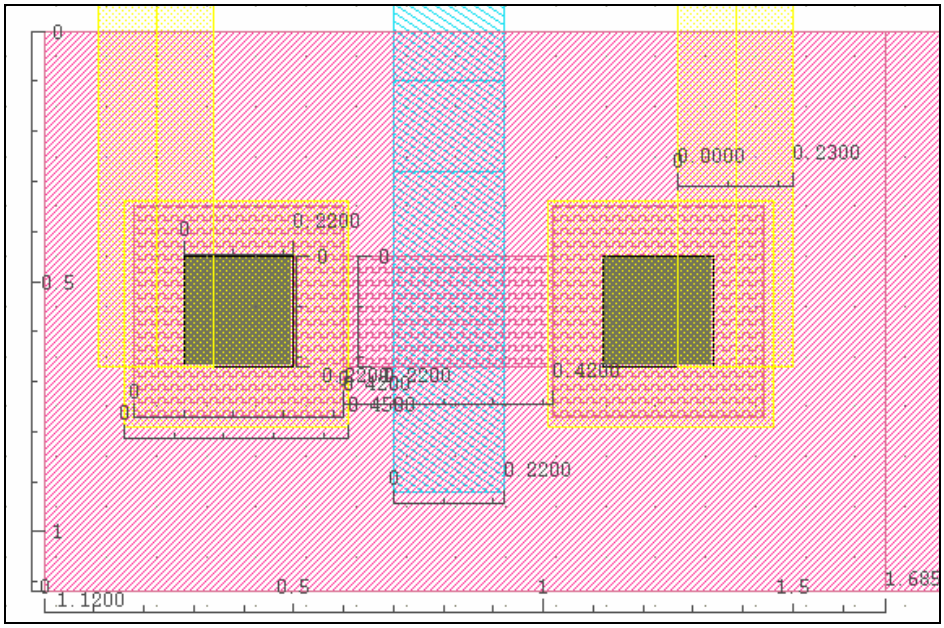

Figure 18: NMOS Layout Measurements

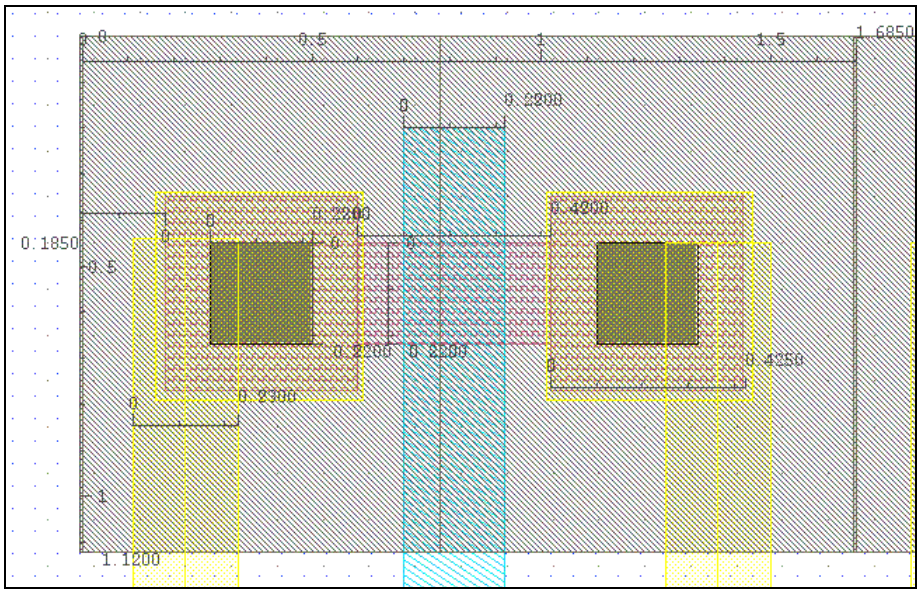

Figure 19: PMOS Layout Measurements

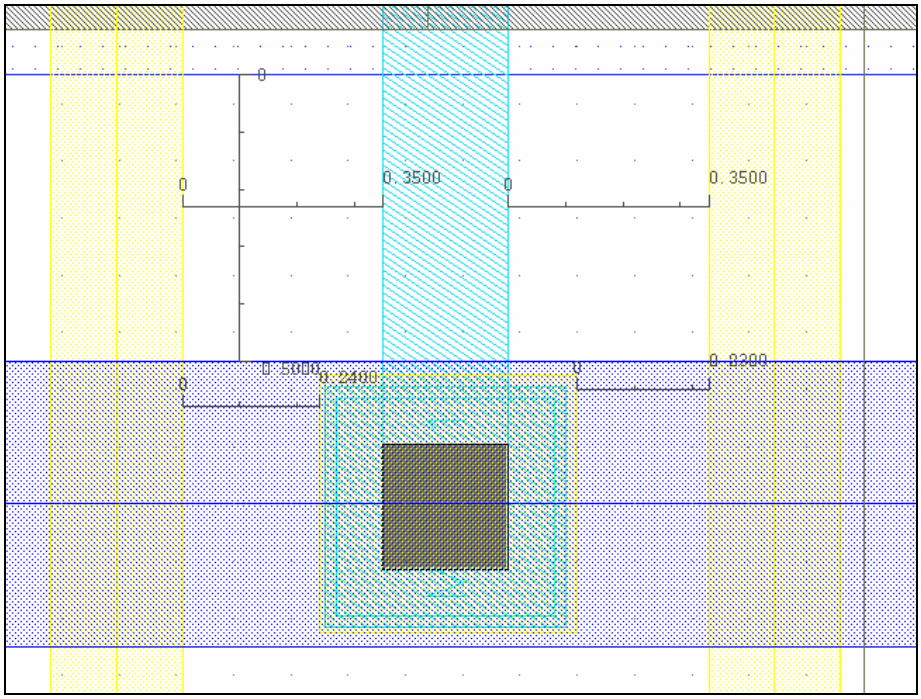

Figure 20: Contact Measurements

The number of transistors and their dimensions are indicated in Table 7 below:

Table 7: Layout Area and Size

Name	Value
Number of transistors	72
Layout Dimensions (W x L)	30.80um x 36.40um = 1.12nm^2
CMOS length/width	0.18um/0.22um

4.2 Simulation of Layout

Final simulation of the layout is displayed in Figure 21 and Figure 22 below. It is noted that parasitic capacitance is extracted and that this model is used for simulation. Due to the amount of signal degradation experienced by the adder at an input voltage at 0.9V, V_{dd} is increased to 1.2V to improve the overall performance of the circuit. This is discussed below.

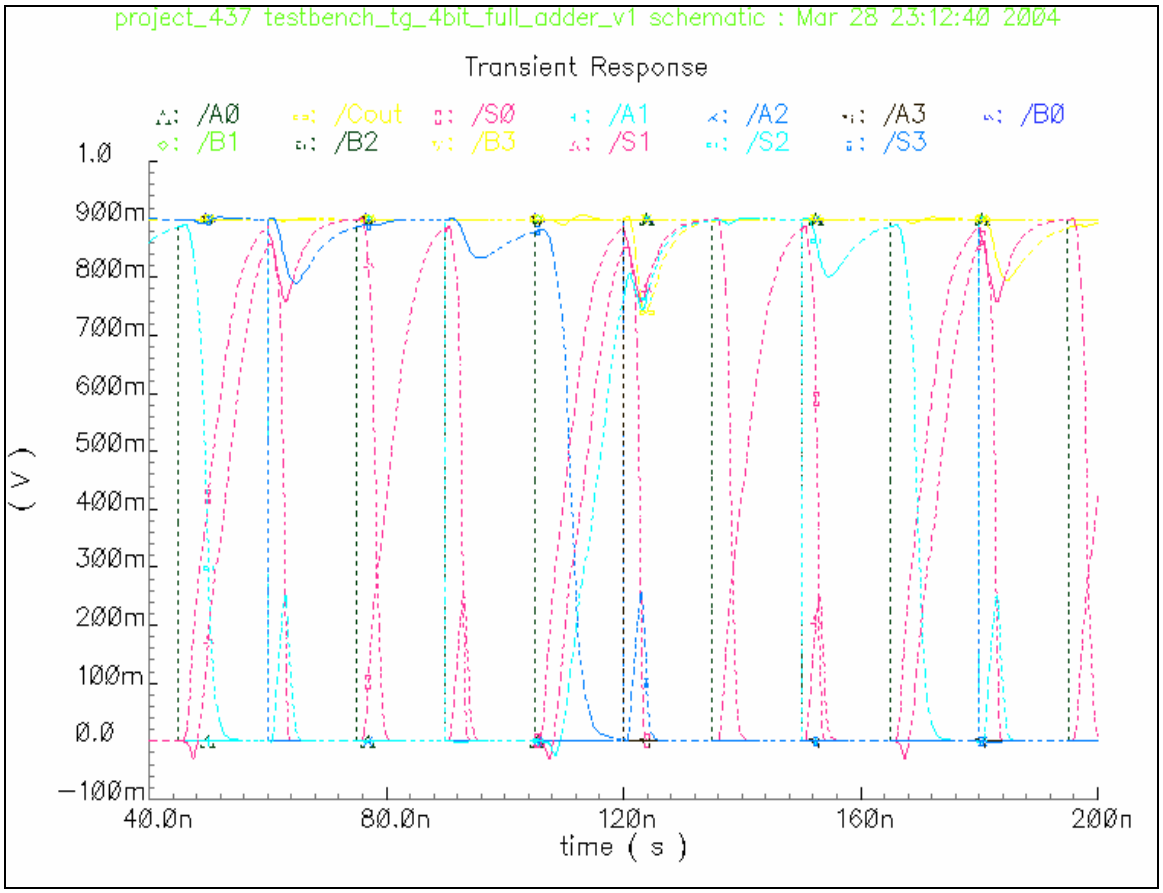

Figure 21: Simulation of Extracted Layout before Adjustment

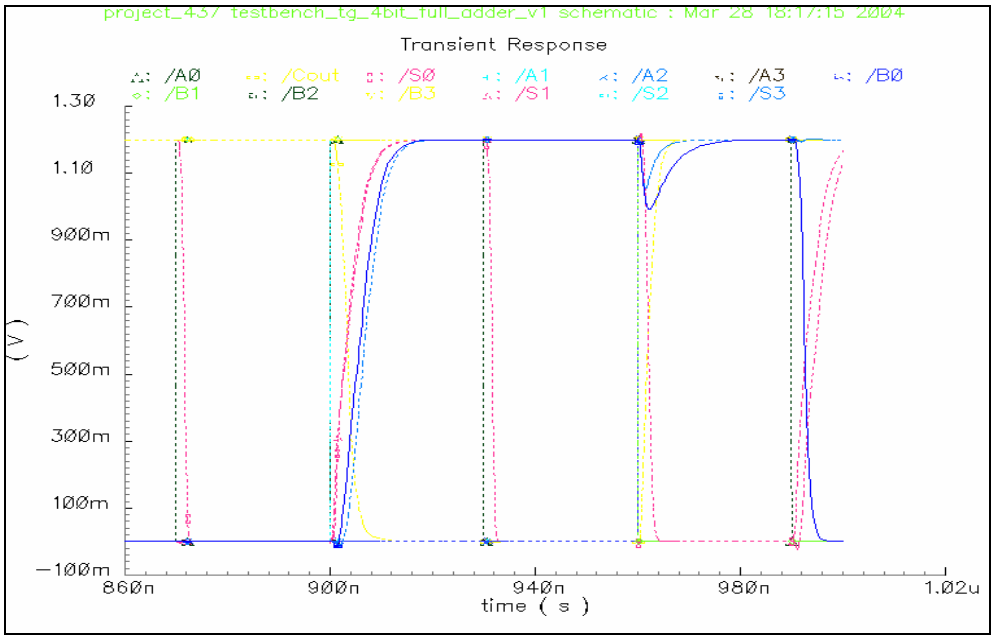

Figure 22: Simulation of Extracted Layout after Adjustment

Table 8: Layout Simulation Data

Controlled Variables:

Variable	Value
V_{dd}	1.2v
Load Capacitance	35f
Input Rise Time	1p
Input Fall Time	1p
Minimum Width	220n
Minimum Length	220n
Input Frequency	16Mhz
Simulation Time	3840n

Observation:

Variable	Value
Rise Time	2.256n
Fall Time	1.73n
Average Input Power	2.95u
Average Device Power	4.98u
Power Dissipation	7.932u
Delay	8.008ns
Power Delay Product	15.9f
Maximum Frequency (1/4*td)	31.12MHz
Figure of Merit (Frequency/Power)	3.92x10^12

Glitch min V

	Falling		Rising	
Signal	**Voltage (mV)**	**Delay (ns)**	**Volt (mV)**	**Delay (ns)**
S0	**-**	**-**	**-**	**-**
S1	**1059**	**6.91**	**230**	**1.96**
S2	**997**	**13.4**	**247**	**2.56**
S3	**961.4**	**6.02**	**261**	**2.34**
C_{out}	**1003**	**8.9**	**265**	**2.46**

With the additional delay produced by parasitic capacitance, performance has deteriorated in comparison to the results obtained from schematic simulation. It appears as though capacitance has significantly diminished the transient response of the circuit as the effects of glitching is especially pronounced in these simulations. Perhaps the channel width should be increased to compensate for this effect. Consequently, to improve the performance of the circuit to acceptable levels, the input/device voltage is regrettably increased. However, power dissipation is still within acceptable limits imposed by the target application; therefore, the slight rise in power dissipation is acceptable. Furthermore, the increase in voltage has significantly restored the waveform back to its original levels of performance as can be seen from schematic results.

5.0 Analysis

Results from the schematic and layout are compared in the next section. In addition, performance is validated against the target application. If the results satisfy the specifications imposed by the target application, then the adder design is acceptable.

5.1 Comparison of Schematic with Layout

Due to the parasitic parameters in the layout, as shown in Figure 21 in the previous section, some signals are distorted to the extend that the waveform is not acceptable. The glitches turn out to have significant effects on the logical function of the 4-bit adder design. This is a potential reason why the power dissipation is increased by 124% as shown in Table 9. Fortunately, the original design is well beyond the requirement of the target application. Some parameters are adjusted to fix the problem. Table 8 shows the parameters and their values that are adjusted.

Table 9 : Comparison of Schematic simulation data and Layout simulation data

Variable	Schematic Simulation	Layout Simulation (Before Adjustment)	Layout Simulation (After Adjustment)
Rise Time	777p	Not Computable	2.256n
Fall Time	734.97p	Not Computable	1.73n
Average Input Power	0.9215u	Not Computable	2.95u
Average Device Power	1.729u	3.415u	4.98u
Power Dissipation	2.6505u	5.941u	7.932u
Delay	3.263n	Not Computable	8.008ns
Power Delay Product	8.64f	Not Computable	15.9f
Maximum Frequency (1/4*td)	76.6MHz	Not Computable	31.12MHz
Figure of Merit (Frequency/Power)	28.9 x10^12	Not Computable	3.92x10^12

The waveform has degraded due to the parasitic capacitance inherent to the extracted layout. The effects of glitch are more prominent in latter simulations thus prompting the input voltage to be increased for proper functionality. However, the increase in voltage is still within the specifications provided by the target application. Power dissipation is still kept to a minimal with the slight rise in voltage; rather, functionality of the adder has been restored. The tradeoff is acceptable.

5.2 Comparison of Layout with Target Application

Validation is achieved by comparing the performance of the 4-bit TG Adder with the technical specifications provided by the GBA. However, the functionality of the adder plays only a small part of the overall GBA device. Thus, it is impossible to state that power consumption of the GBA rests entirely on a single 4-bit adder thus undermine the comparison altogether. On contrary, the assumption that the technical specifications of the GBA form the lower bound for the values obtained by the 4-bit Adder is valid. Thus, it is possible to state that by ensuring extremely low power consumption by the adder to almost negligible levels with respect to the overall device, the adder design is validated although the degree at which this is accomplished is impossible to determine. The comparison between the adder and GBA are shown below.

Table 10: Comparison between 4-bit TG Adder Performance with Target Application

Performance Metrics	Technical Specifications of the GBA	Simulation Results of the 4-bit TG Adder
CPU	32-bit RISC-CPU + 8-bit CISC-CPU	N/A
Power Supply	2 x Ni-Cd AA @1.2V/1000mAh	1 x Ni-Cd @ 1.2V/1000mAh
Expected Days of Operation	~15 hours	(1Ah/(7.932e-6W/1.2V))=~**17.27 yrs**
Operating Frequency	16 MHz	16MHz
Operating Voltage	<3V	1.2 V

The expected days of operation using relatively the same battery capacity operating at half the input voltage results in an adder that is capable of constant calculation for 17.27 years – which is significantly larger than the number of hours the GBA is able to sustain constant operation. Therefore, the 4-bit TG ripple carry adder has achieved the design objective of low power dissipation with respect to the overall operation of the device.

6.0 Conclusion

The 4-bit TG ripple carry adder has been successfully implemented from schematic design to layout. Simulation data shows acceptable results while maintaining low power dissipation at a reasonable operating frequency. Low power consumption is validated and put into perspective with the GBA target application.

References

Low-Power Digital VLSI Design Circuits and Systems, Mohamed I. Elmasry, Abdellatif Bellaouar